AMENDMENTS TO THE CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. (Original) A test circuit for testing a match detection circuit, said test circuit comprising:

    a test line for providing a load to the match detection circuit, said test line being switchably coupled to a first line of the match detection circuit to provide the load on the first line and to test a feature of the match detection circuit.

2. (Original) The test circuit of claim 1, wherein said first line of said match detection circuit comprises:

    a matchline.

3. (Original) The test circuit of claim 1, wherein said first line of said match detection circuit comprises:

    a discharge line.

4. (Original) The test circuit of claim 1, wherein said test line comprises:

    a test line switch coupled between said load and said match detection circuit.

5. (Original) The test circuit of claim 4, further comprising:

    a test circuit controller for controlling said switch.

6. (Original) The test circuit of claim 4, wherein said load is a resistor.

7. (Original) The test circuit of claim 1, further comprising:

a second test line for providing a second load to the match detection circuit, said second test line being switchably coupled to the first line of the match detection circuit to provide the second load on the first line to test a feature of the match detection circuit.

8. (Original) The test circuit of claim 7, wherein said second load is different from said first load.

9. (Original) The test circuit of claim 7, further comprising:

a third test line for providing a third load to the match detection circuit, said third test line being switchably coupled to the first line of the match detection circuit to provide the third load on the first line to test a feature of the match detection circuit.

10. (Original) The test circuit of claim 9, wherein said third load is different from said first load.

11. (Original) The test circuit of claim 10, wherein said third load is different from said second load.

12. (Original) A test circuit for a detection match circuit, said test circuit comprising:

a test line being switchably coupled to a first line of a match detection circuit for providing a load to said match detection circuit.

13. (Original) The test circuit of claim 12, wherein said test line comprises:

a load; and

a test line transistor coupled between said load and said match detection circuit.

14. (cancelled).

15. (Original) The test circuit of claim 14, wherein said load further comprises a voltage, wherein said voltage is coupled to said test line transistor through said resistor.

16. (Original) The test circuit of claim 14, wherein said load further comprises a ground potential, wherein said ground potential is coupled to said test line transistor through said resistor.

17. (Original) The test circuit of claim 12, wherein said first line of said match detection circuit is a matchline.

18. (Original) The test circuit of claim 12, wherein said first line of said match detection circuit is a discharge line.

19. (Original) The test circuit of claim 12 further comprising:

a test circuit controller coupled to the gate of said test line transistor through a test control line for activating said test line transistor.

20. (Original) The test circuit of claim 19 further comprising:

a decision circuit for receiving input from said test control line for determining if said test control line has been enabled and outputting a circuit enable signal reflecting the results of said determination, said enable signal adapted to be received by a gate of transistor in between said discharge line and ground, said decision circuit coupled to said test control line.

21. (Original) The test circuit of claim 20, where said decision circuit comprises a NOR circuit.

22. (Original) A test circuit for a match detection circuit, said test circuit comprising:

a test circuit for providing a first load to said match detection circuit to test a margin of said match detection circuit.

23. (Original) The test circuit of claim 22, wherein said test circuit further comprises:

a first test line for providing said first load to said match detection circuit.

24. (Original) The test circuit of claim 23, wherein said test circuit further comprises:

a second test line for providing a second load to said match detection circuit.

25. (Original) The test circuit of claim 24, wherein said second load has a different load value than a load value of said first load.

26. (Original) The test circuit of claim 24, wherein said test circuit further comprises:

a test line transistor for switchably coupling said test line to said match detection circuit, wherein one of said source/drain regions of said test line transistor is coupled to said match detection circuit, the other of said source/drain regions of said test line transistor is coupled to a load.

27. (Original) The test circuit of claim 26, wherein said test circuit further comprises:

a test circuit controller for controlling said first load provided to said match detection circuit, said test circuit controller coupled to said gate of said test line transistor.

28. (Original) The test circuit of claim 22, wherein said test circuit is switchably coupled to a matchline of said match detection circuit.

29. (Original) The test circuit of claim 22, wherein said test circuit is switchably coupled to a discharge line of said match detection circuit.

30. (Original) A test circuit for testing a match detection circuit, said test circuit comprising:

a test circuit controller;

a plurality of test lines switchably coupled to a matchline of said match detection circuit to test a feature of said match detection circuit, wherein each of said plurality of test lines comprises:

a load, wherein said load is a resistor; and

a test line transistor coupled between said load and said matchline, a gate of said test line transistor coupled to said test circuit controller.

31. (Original) A test circuit for testing a match detection circuit, said test circuit comprising:

a test circuit controller;

a plurality of test lines switchably coupled to a matchline of said match detection circuit to test a feature of said match detection circuit, wherein each of said plurality of test lines comprises:

a load, wherein said load is a voltage; and a test line transistor coupled between said load and said matchline, a gate of said test line transistor coupled to said test circuit controller

32. (Original) A test circuit for testing a match detection circuit, said test circuit comprising:

a test circuit controller;

a decision circuit;

a plurality of test lines switchably coupled to a discharge line of said match detection circuit to test a feature of said match detection circuit, wherein each of said plurality of test lines comprises:

a load, wherein said load is a resistor; and

a test line transistor coupled between said load and said discharge line, a gate of said test line transistor mutually coupled to said test circuit controller and said decision circuit.

33. (Original) A router, comprising:

a content addressable memory (CAM) system, said CAM system comprising:

a test circuit for testing a match detection circuit, said test circuit comprising:

a test circuit controller;

a plurality of test lines switchably coupled to a matchline of said match detection circuit to test a feature of said match detection circuit, wherein each of said plurality of test lines comprises:

a load, wherein said load is a resistor; and

a test line transistor coupled between said load and said matchline, a gate of said test line transistor coupled to said test circuit controller.

34. (Original) A router, comprising: a content addressable memory (CAM) system, said CAM system comprising:

a test circuit for testing a match detection circuit, said test circuit comprising:

a test circuit controller;

a plurality of test lines switchably coupled to a matchline of said match detection circuit to test a feature of said match detection circuit, wherein each of said plurality of test lines comprises:

a load, wherein said load is a voltage; and

a test line transistor coupled between said load and said matchline, a gate of said test line transistor coupled to said test circuit controller.

35. (Original) A router, comprising:

a content addressable memory (CAM) system, said CAM system comprising:

a test circuit for testing a match detection circuit, said test circuit comprising:

a test circuit controller;

a decision circuit;

a plurality of test lines switchably coupled to a discharge line of said match detection circuit to test a feature of said match detection circuit, wherein each of said plurality of test lines comprises:

a load, wherein said load is a resistor; and

a test line transistor coupled between said load and said discharge line, a gate of said test line transistor mutually coupled to said test circuit controller and said decision circuit.

36. (Original) A integrated circuit chip, comprising:

a content addressable memory (CAM) system, said CAM system comprising:

a test circuit for testing a match detection circuit, said test circuit comprising:

a test circuit controller;

a plurality of test lines switchably coupled to a matchline of said match detection circuit to test a feature of said match detection circuit, wherein each of said plurality of test lines comprises:

a load, wherein said load is a resistor; and

a test line transistor coupled between said load and said matchline, a gate of said test line transistor coupled to said test circuit controller.

37. (Original) A integrated circuit chip, comprising:

a content addressable memory (CAM) system, said CAM system comprising:

a test circuit for testing a match detection circuit, said test circuit comprising: a test circuit controller;

a plurality of test lines switchably coupled to a matchline of said match detection circuit to test a feature of said match detection circuit, wherein each of said plurality of test lines comprises:

a load, wherein said load is a voltage; and

a test line transistor coupled between said load and said matchline, a gate of said test line transistor coupled to said test circuit controller.

38. (Original) A integrated circuit chip, comprising:

a content addressable memory (CAM) system, said CAM system comprising:

a test circuit for testing a match detection circuit, said test circuit comprising:

a test circuit controller;

a decision circuit;

a plurality of test lines switchably coupled to a discharge line of said match detection circuit to test a feature of said match detection circuit, wherein each of said plurality of test lines comprises:

a load, wherein said load is a resistor; and

a test line transistor coupled between said load and said discharge line, a gate of said test line transistor mutually coupled to said test circuit controller and said decision circuit.

39. (Original) A processor system, comprising:

a processor;

a content addressable memory (CAM) system, said CAM system comprising:

a test circuit for testing a match detection circuit, said test circuit comprising:

a test circuit controller;

a plurality of test lines switchably coupled to a matchline of said match detection circuit to test a feature of said match detection circuit, wherein each of said plurality of test lines comprises:

a load, wherein said load is a resistor; and

a test line transistor coupled between said load and said matchline, a gate of said test line transistor coupled to said test circuit controller.

40. (Original) A processor system, comprising:

a processor; a content addressable memory (CAM) system, said CAM system comprising:

a test circuit for testing a match detection circuit, said test circuit comprising:

a test circuit controller;

a plurality of test lines switchably coupled to a matchline of said match detection circuit to test a feature of said match detection circuit, wherein each of said plurality of test lines comprises:

a load, wherein said load is a voltage; and

a test line transistor coupled between said load and said matchline, a gate of said test line transistor coupled to said test circuit controller.

41. (Original) A processor system, comprising:

a processor;

a content addressable memory (CAM) system, said CAM system comprising:

a test circuit for testing a match detection circuit, said test circuit comprising:

a test circuit controller;

a decision circuit;

a plurality of test lines switchably coupled to a discharge line of said match detection circuit to test a feature of said match detection circuit, wherein each of said plurality of test lines comprises:

a load, wherein said load is a resistor; and

a test line transistor coupled between said load and said discharge line, a gate of said test line transistor mutually coupled to said test circuit controller and said decision circuit.

42. (Original) A method of testing a match detection circuit, comprising the steps of:

switchably coupling a load to said match detection circuit; and

applying said load to said match detection circuit to test a feature of the match detection circuit.

43. (Original) The method of claim 42, further comprising:

comparing a stored data bit in said match detection circuit with a comparand data bit.

44. (Original) The method of claim 42, wherein said step of switching further comprises:

applying resistance to a first line of said match detection circuit.

45. (Original) The method of claim 42, wherein said step of switching further comprises:

applying voltage to a first line of said match detection circuit.

46. (Original) The method of claim 44, wherein said first line is a matchline.

47. (Original) The method of claim 45, wherein said first line is a matchline.

48. (Original) The method of claim 45, wherein said first line is a discharge line.

49. (Original) A method of testing a match detection circuit, comprising the step of:

precharging a matchline of said match detection circuit;

applying a load to said matchline to test a feature of the match detection circuit;

comparing a stored bit in said match detection circuit with a comparand bit; and

determining whether said matchline is pulled to ground when a mismatch occurs in said comparing step.

50. (Original) The method of claim 49, wherein said applying step comprises:

applying a voltage to said matchline of said match detection circuit.

51. (Original) The method of claim 49, further comprising the step of :

applying a second load to said matchline of said match detection circuit.

52. (Original) The method of claim 51, further comprising the step of :

applying a third load to said matchline of said match detection circuit.

53. (Original) A method of testing a match detection circuit, comprising the step of:

precharging a matchline of said match detection circuit;

applying a load to said matchline to test a feature of the match detection circuit;

comparing a stored bit in said match detection circuit with a comparand bit; and

determining whether said matchline is pulled to ground when a match occurs in said comparing step.

54. (Original) The method of claim 53, wherein said applying step comprises applying a ground potential to said matchline of said match detection circuit.

55. (Original) The method of claim 54, further comprising the step of :

applying a second load to said matchline of said match detection circuit.

56. (Original) The method of claim 55, further comprising the step of :

applying a third load to said matchline of said match detection circuit.

57. (Original) A method of testing a match detection circuit, comprising the steps of:

precharging a matchline of said match detection circuit;

applying a load to a discharge line to test a feature of the match detection circuit;

comparing a stored bit in said match detection circuit with a comparand bit; and

determining whether said matchline is pulled to ground when a mismatch occurs in said comparing step.

58. (Original) The method of claim 57, wherein said applying step comprises:

applying a ground potential to said discharge line of said match detection circuit.

59. (Original) The method of claim 57, further comprising the step of :

applying a second load to said discharge line of said match detection circuit.

60. (Original) The method of claim 59, further comprising the step of :

applying a third load to said discharge line of said match detection circuit.

61. (New) A content addressable memory, comprising:

a match detection circuit coupled to a match line and a discharge line; and

a test circuit for testing said match detection circuit, said test circuit comprising:

at least one test line for testing a feature of said match detection circuit, wherein said test line comprises:

a resistance; and

a test line transistor for selectively coupling said resistance between said matchline and a voltage source line.

62. (New) The content addressable memory of claim 61, further comprising:

a plurality of test lines having respective resistances.

63. (New)A content addressable memory, comprising:

a match detection circuit coupled to a match line and a discharge line; and

a test circuit for testing said match detection circuit, said test circuit comprising:

at least one test line for testing a feature of said match detection circuit, wherein said test line comprises:

a resistance; and

a test line transistor for selectively coupling said resistance between said match line and a ground line.

64. (New) The content addressable memory of claim 61, further comprising:

a plurality of test lines having respective resistances.

65. (New)A content addressable memory, comprising:

a match detection circuit coupled to a match line and a discharge line; and

a test circuit for testing said match detection circuit, said test circuit comprising:

at least one test line for testing a feature of said match detection circuit, wherein said test line comprises:

a resistance; and

a test line transistor for selectively coupling said resistance between said discharge line and a ground line.

66. (New) The content addressable memory of claim 61, further comprising:

a plurality of test lines having respective resistances.